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Capacitor unbalance protection for blocks in bridge connection

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User's manual version information

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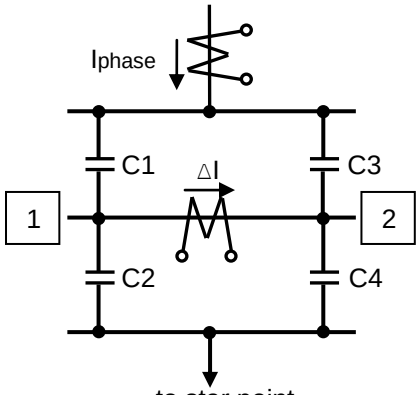
Capacitor unbalance protection function for blocks in bridge connection

This version of the capacitor unbalance protection can be applied if the capacitors in the phases are arranged in bridge connection (“H configuration”), according to Figure below.



(drawing in one phase only)

The capacitors in each phase are arranged in two branches with a current transformer connected between midpoints or close to midpoints of the two branches. Failures anywhere in the branches will cause an unbalance current to flow through the current transformer.

This method is suitable for large capacitor banks since the total bank will be divided into separate protection zones. The method is not influenced by phase voltage unbalances. It may be used in delta- or star-connected banks with the neutral grounded or ungrounded.

The shunt capacitor banks are usually constructed of capacitor units, and the units contain capacitor elements.

There are constructions of the bank where fuses are connected inside a capacitor unit, in series with an element or a group of elements. The fuse is connected in series with the element that the fuse is designed to isolate if the element becomes faulty. After the breakdown of an element, the fuse connected to it will blow and isolate it from the remaining part of the capacitor, which allows the unit to continue in service. The blowing of one or more fuses decreases the capacitance value and additionally it will cause voltage changes within the bank.

If no internal fuses are applied then the breakdown of an element increases the capacitance value and additionally it will cause voltage changes within the bank.

Each time an internal capacitor element fails, a slight change of voltage distribution and current flow within the capacitor bank is encountered. The magnitude of these changes depends upon the number of failed elements and their location within the bank.

The main purpose of the capacitor unbalance protection is to give an alarm or to disconnect the entire capacitor bank when unbalances across healthy capacitors, adjacent to a failed capacitor, are excessive. Normally not more than 10 % unbalance should be allowed (unbalance limit according to (IEC 60871-1 Shunt capacitors for a.c. power systems having a rated voltage above 1000 V - Part 1: General).

If an externally fused capacitor is disconnected by its fuse, a larger voltage and current change is obtained than if single elements are disconnected by internal fuses.

This kind of protection prevents steady-state overvoltage and accelerated aging of the capacitor elements.

Another function of the unbalance protection is to remove the bank from service for a fault not isolated by a fuse or to protect banks that are not internally or externally fused. Unbalance protection is not a replacement for short-circuit protection.

The related standard permits a considerable amount of asymmetry, which can be up to 10%, consequently in healthy state a relatively high current can flow through the current transformer. At commissioning the unbalance protection function stores the vector position and the value of the "natural" unbalance currents as three reference currents $\Delta Iref$ and additionally those of one of the phase currents $Iphase_{ref}$ *(= IL1).*

The reference currents are corrected according to the actually measured phase currents *Iphase* and the stored $Iphase_{ref}$ reference phase current.

$$\mathbf{\Delta}Iref_{corr} = \Delta Iref \frac{Iphase}{Iphase_{ref}}$$

where all current values are complex Fourier base harmonic vectors for the phases individually:

$\Delta Iref$	reference current measured in the bridge of all three phases at commissioning,
$\Delta Iref_{corr}$	corrected reference currents of all three phases,
Iphase	measured phase current of one of the three phases (*IL1)*,
$Iphase_{ref}$	phase current of one of the three phases measured at commissioning (*IL1).*

The correction is performed with one phase current in all three phases separately.

NOTE: This approach using a single phase current supposes that the asymmetry of the network itself does not change, or the changes are cleared with high speed by other protection functions. If considerable steady-state changes in the symmetry of the network are expected, then the measurement and correction based a single phase current is not sufficient. In this case please consult Protecta Co. Ltd. for solution.

If there are no changes inside the capacitor then no change can be detected in the actually measured unbalance current related to the corrected reference current.

Accordingly the energizing quantity for evaluation is the difference of the measured currents in the bridges and the corrected reference current:

$$G = dI = \Delta I - \mathbf{\Delta}Iref_{corr}$$

where all current values are complex Fourier base harmonic vectors:

ΔI	currents measured in the bridge,
$\Delta Iref_{corr}$	corrected reference currents (see above).

NOTE: The correction is performed in all three phases separately with one phase current.

This is the task of the commissioning to store the reference values for the bridge currents $\Delta Iref$, and that of one of the phase currents $Iphase_{ref}$ in the memory.

For this purpose the function block has a dedicated binary input: *Calib*. This input must be activated for the calibration. For the physical means for activation see the description of the configuration. This input may be programmed by the user using the graphic logic editor.

The calibration at the moment of activation can be performed only if the conditions for calibration are fulfilled. The conditions for calibration are:

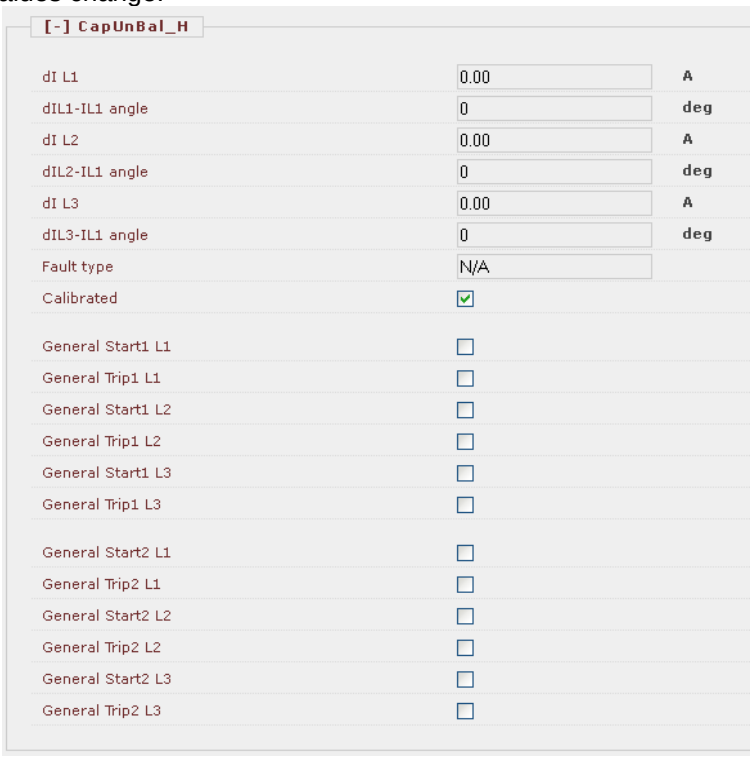
- The phase currents have to be less than 2*In of the current input,
- The phase currents have to be above 70% of the rated capacitor current,
- The bridge currents have to be less than the value set by the dedicated parameter.

The calibrated state is indicated by the dedicated binary output of the function *Calibrated*. This output gets in “true” state only if the calibration procedure in all three phases was successful.

The calibration values are stored in non-volatile memory, separately for each parameter set.

The *Reset* binary input resets the calibrated state.

Among the “on-line” information the function continuously displays the ΔI currents and their angles measured in the bridges. At the moment of calibration this vectors reset to zero vector (see Figure below, dI=ΔI). At the same time the “*Calibrated*” field on the screen displays a check-mark. If however after calibration any changes happen within the capacitor bank then the displayed values change.



The capacitor unbalance protection function is configured with two independent stages.

For the first stage definite time characteristic and several types of inverse characteristics can be selected.

The second stage has a definite time characteristic.

The inverse time operating characteristics are defined by the formula below:

$$t(G) = TMS\left[\frac{k}{\left(\frac{G}{G_S}\right)^{\alpha} - 1} + c\right] \text{ when } G > G_S$$

where

t(G)(seconds)	theoretical operate time with constant value of *G*,
k, c	constants characterizing the selected curve (in seconds),
α	constants characterizing the selected curve (no dimension),
G	measured value of the characteristic quantity, Fourier base harmonic value, see section 1.2.3,
G_S	preset starting value of the characteristic quantity,
TMS	preset time multiplier (no dimension).

The constant values k, c and α of the standard dependent time characteristics, see below.

	IEC ref	Title	k_r	c	α
1	A	IEC Inv	0,14	0	0,02
2	B	IEC VeryInv	13,5	0	1
3	C	IEC ExtInv	80	0	2
4		IEC LongInv	120	0	1
5		ANSI Inv	0,0086	0,0185	0,02
6	D	ANSI ModInv	0,0515	0,1140	0,02
7	E	ANSI VeryInv	19,61	0,491	2
8	F	ANSI ExtInv	28,2	0,1217	2
9		ANSI LongInv	0,086	0,185	0,02
10		ANSI LongVeryInv	28,55	0,712	2
11		ANSI LongExtInv	64,07	0,250	2

The end of the effective range of the inverse time characteristics (G_D) is:

$$G_D = 20 * G_S$$

Above this value the theoretical operating time is definite:

$$t(G) = TMS\left[\frac{k}{\left(\frac{G_D}{G_S}\right)^{\alpha} - 1} + c\right] \text{ when } G > G_D = 20 * G_S$$

Additionally a minimum time delay can be defined by parameter setting. This delay is valid if it is longer than t(G), defined by the formula of the operating characteristics above.

The inverse characteristic is valid above G_T =1,1* G_s. Above this value the function is guaranteed to operate.

Resetting characteristics of the inverse time delay is as follows.

- For IEC type characteristics the resetting is after a fix time delay defined by the parameter CapUnB1_Reset_TPar_ (Reset Time),
- for ANSI types however according to the formula below:

$$t_r(G) = TMS\left[\frac{k_r}{1 - \left(\frac{G}{G_S}\right)^{\alpha}}\right] \text{ when } G < G_S$$

where

$t_r(G)$(seconds)	theoretical reset time with constant value of *G*,
k_r	constants characterizing the selected curve (in seconds),
α	constants characterizing the selected curve (no dimension),
G	measured value of the characteristic quantity, Fourier base harmonic of the phase currents, see section 1.2.3,
G_S	preset starting value of the characteristic quantity (CapUnB3_StCurr1_IPar_, Start current 1),
TMS	preset time multiplier (no dimension).

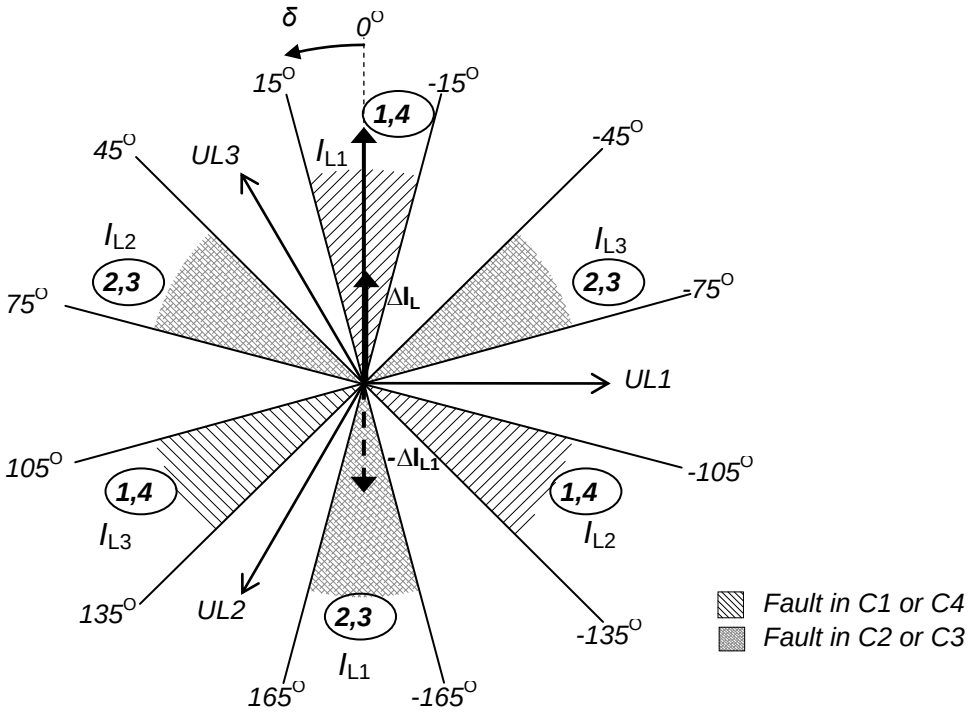
The resetting constants of the standard dependent time characteristics are shown below.

	IEC ref	Title	k_r	α
1	A	IEC Inv	Resetting after fix time delay, according to preset parameter CapUnB3_Reset_TPar_ "Reset Time"	
2	B	IEC VeryInv		
3	C	IEC ExtInv		
4		IEC LongInv		
5		ANSI Inv	0,46	2
6	D	ANSI ModInv	4,85	2
7	E	ANSI VeryInv	21,6	2
8	F	ANSI ExtInv	29,1	2
9		ANSI LongInv	4,6	2
10		ANSI LongVeryInv	13,46	2
11		ANSI LongExtInv	30	2

Fault location

The vector measurement enables identification of the faulty capacitor unit. For the explanation of the principle of fault location consider the positive direction of the current I_{phase} and ΔI as indicated in Figure above, the current ΔI flows from capacitor unit 1 to capacitor unit 2.

Now consider a fault in phase L1, inside unit 1 in the capacitor C1, which increases the capacitance value, consequently decreases the impedance related to the impedance of C3. The current in C1 increases related to the current of C3, consequently the current flows from the unit 1 towards the unit 2. It is obvious that this current is in phase with the current of the original phase capacitor "*IL1*", as it is indicated in Figure below. Consequently the Δ*I* current measured in the bridge is in phase with the current of the original phase capacitor. To permit some asymmetry changes in the network and some measuring error, this current is inside the shaded area between -15 ° and +15 °. The on-line measurement will display the increased "*dI*" value with "*dI-IL1 angle*" in this range. The related event indicates "L1-1". The same current vector flows if the value of the capacitor 4 increases, here the event should be "L1-4". Based on the current measurement these two events cannot be separated so the common fault identification is: " L1-1 or L1-4"



If the capacitor elements are not fused then the breakdown of a capacitor element will short-circuit a “layer” of capacitors. The capacitance increases and consequently also the capacitive current increases. This case was described in the explanation above.

If however the capacitor elements are individually fused then the breakdown of a capacitor element is disconnected from the “layer” of capacitors. The resultant capacitance decreases, and the result is opposite to the explanation in Figure above.

For correct evaluation the information is needed: whether internal fuses are applied or not. This is to be set by the Boolean parameter *Internal fuse*.

The event list related to the capacitor faults can contain the following messages:

Message	Explanation
L1-1 or L1-4	Fault in phase L1, C1 or C4
L2-1 or L2-4	Fault in phase L2, C1 or C4
L3-1 or L3-4	Fault in phase L3, C1 or C4
L1-2 or L1-3	Fault in phase L1, C2 or C3
L2-2 or L2-3	Fault in phase L2, C2 or C3
L3-2 or L3-3	Fault in phase L3, C2 or C3

NOTE: The fault location is active in “*Calibrated*” state only. The event is registered at the moment of trip command generation.

Technical data

Function	Value	Accuracy
Pick-up starting accuracy	$20 \le G_S \le 1000$	< 5 %
Pickup time	< 40 ms	
Angle accuracy		<1 degree
Reset ratio	0,9	
Reset time Dependent time char. Definite time char.	 approx 60 ms	< 2% or ±35 ms, whichever is greater
Operate time accuracy		±5% or ±15 ms, whichever is greater

Parameters

Enumerated parameters

Parameter name	Title	Selection range	Default
Enabling or disabling the capacitor unbalance protection function			
CapUnB3_Oper1_EPar_	Operation Stage 1	Off, DefinitTime, IEC Inv, IEC VeryInv, IEC ExtInv, IEC LongInv, ANSI Inv, ANSI ModInv, ANSI VeryInv, ANSI ExtInv, ANSI LongInv, ANSI LongVeryInv, ANSI LongExtInv	Off
CapUnB3_Oper2_EPar_	Operation Stage2	Off, On	Off

Boolean parameters

Parameter name	Title	Default	Explanation
CapUnB3_IntFuse_BPar_	Internal fuse	0	0 means no internal fuse 1 means capacitor units with internal fuse

Integer parameter

Parameter name	Title	Unit	Min	Max	Step	Default
Current setting for the capacitor unbalance protection function, first stage						
CapUnB3_StCurr1_IPar_	Start Current 1	%	10	100	1	10
Current setting for the capacitor unbalance protection function, second stage						
CapUnB3_StCurr2_IPar_	Start Current 2	%	5	100	1	10
Nominal current of the capacitor, as percent of the rated input current						
CapUnB3_NomCurr_IPar_	Inom capacitor	%	15	120	1	100
ΔI setting, at calibration the current in the bridge must be below this level						
CapUnB3_dIMax_IPar_	dI maxcalib	%	5	50	1	10

Float point parameter

Parameter name	Title	Dim.	Min	Max	Default
Time multiplier setting for the inverse type characteristics					
CapUnB3_Multip_FPar_	Time Multiplier	sec	0.05	999	1.0

Timer parameters

Parameter name	Title	Unit	Min	Max	Step	Default
Minimum time delay for the inverse type characteristics, first stage (valid, if this characteristic is selected)						
CapUnB3_MinDel_TPar_	Min Time Delay	msec	0	60000	1	100
Definite time delay for the first stage (valid, if this characteristic is selected)						
CapUnB3_DefDel_TPar_	Definite Time Delay	msec	0	60000	1	1000
Reset time setting, first stage						
CapUnB3_Reset_TPar_	Reset Time	msec	0	60000	1	100
Definite time delay for the second stage						
CapUnB3_Delay2_TPar_	Delay Stage 2	msec	0	60000	1	1000

Binary output status signals

Binary output status signals	Signal title	Explanation
CapUnB3_GenSt1L1_GrI_	General Start 1 L1	General start signal for stage 1 phase L1
CapUnB3_GenTr1L1_GrI_	General Trip 1 L1	General trip command for stage 1 phase L1
CapUnB3_GenSt2L1_GrI_	General Start 2 L1	General start signal for stage 2 phase L1
CapUnB3_GenTr2L1_GrI_	General Trip 2 L1	General trip command for stage 2 phase L1
CapUnB3_GenSt1L2_GrI_	General Start 1 L2	General start signal for stage 1 phase L2
CapUnB3_GenTr1L2_GrI_	General Trip 1 L2	General trip command for stage 1 phase L2
CapUnB3_GenSt2L2_GrI_	General Start 2 L2	General start signal for stage 2 phase L2
CapUnB3_GenTr2L2_GrI_	General Trip 2 L2	General trip command for stage 2 phase L2
CapUnB3_GenSt1L3_GrI_	General Start 1 L3	General start signal for stage 1 phase L3
CapUnB3_GenTr1L3_GrI_	General Trip 1 L3	General trip command for stage 1 phase L3
CapUnB3_GenSt2L3_GrI_	General Start 2 L3	General start signal for stage 2 phase L3
CapUnB3_GenTr2L3_GrI_	General Trip 2 L3	General trip command for stage 2 phase L3
CapUnB1_Calib_GrI_	Calibrated	True, if the function has been calibrated

Binary input status signals

The conditions of the binary input signals are defined by the user, applying the graphic logic editor.

Binary input status signals	Signal title	Explanation
CapUnB3_Reset_GrO_	Reset	Resetting the calibrated state
CapUnB3_Calibr_GrO_	Calibr	Binary input for calibration
CapUnB3_Blk_GrO_	Blk	Blocking input