

FUNCTION BLOCK DESCRIPTION

Capacitor unbalance protection for blocks in bridge connection

ANSI 51NC





VERSION INFORMATION

VERSION	DATE	MODIFICATION	COMPILED BY
1.0	2012-02-01	First edition	Petri
1.1	2015-12-07	Minor correction and rearrangement	Petri
2.0	2024-07-31	New documentation design, new chapters, figures, data updated, graphical analogue inputs introduced, IEC61850 info added	Ádám, Erdős

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USED SYMBOLS



Additional information



Useful information for settings.



Important part for proper usage.

1 Operation principle

1.1 Application

The shunt capacitor banks are usually constructed of capacitor units, and the units contain capacitor elements.

There are constructions of the bank where fuses are connected inside a capacitor unit, in series with an element or a group of elements. The fuse is connected in series with the element that the fuse is designed to isolate if the element becomes faulty. After the breakdown of an element, the fuse connected to it will blow and isolate it from the remaining part of the capacitor, which allows the unit to continue in service. The blowing of one or more fuses decreases the capacitance value and additionally it will cause voltage changes within the bank.

If no internal fuses are applied, then the breakdown of an element increases the capacitance value and additionally it will cause voltage changes within the bank.

Each time an internal capacitor element fails, a slight change of voltage distribution and current flow within the capacitor bank is encountered. The magnitude of these changes depends upon the number of failed elements and their location within the bank.

The main purpose of the capacitor unbalance protection is to give an alarm or to disconnect the entire capacitor bank when unbalances across healthy capacitors, adjacent to a failed capacitor, are excessive. Normally not more than 10 % unbalance should be allowed (unbalance limit according to IEC 871-1 Shunt capacitors for a.c. power systems having a rated voltage above 1000V – Part 1: General).

If an externally fused capacitor is disconnected by its fuse, a larger voltage and current change is obtained than if single elements are disconnected by internal fuses.

This kind of protection prevents steady-state overvoltage and accelerated aging of the capacitor elements.

Another function of the unbalance protection is to remove the bank from service for a fault not isolated by a fuse or to protect banks that are not internally or externally fused. Unbalance protection is not a replacement for short-circuit protection.

1.2 Mode of operation

1.2.1 Construction of the capacitor bank

This version of the capacitor unbalance protection can be applied if the capacitors in the phases are arranged in bridge connection ("H configuration"), according to Figure 1-1.

The capacitors in each phase are arranged in two branches with a current transformer connected between midpoints or close to midpoints of the two branches. Failures anywhere in the branches will cause an unbalance current to flow through the current transformer.

This method is suitable for large capacitor banks since the total bank will be divided into separate protection zones. The method is not influenced by phase voltage unbalances. It may be used in delta- or star-connected banks with the neutral grounded or ungrounded.

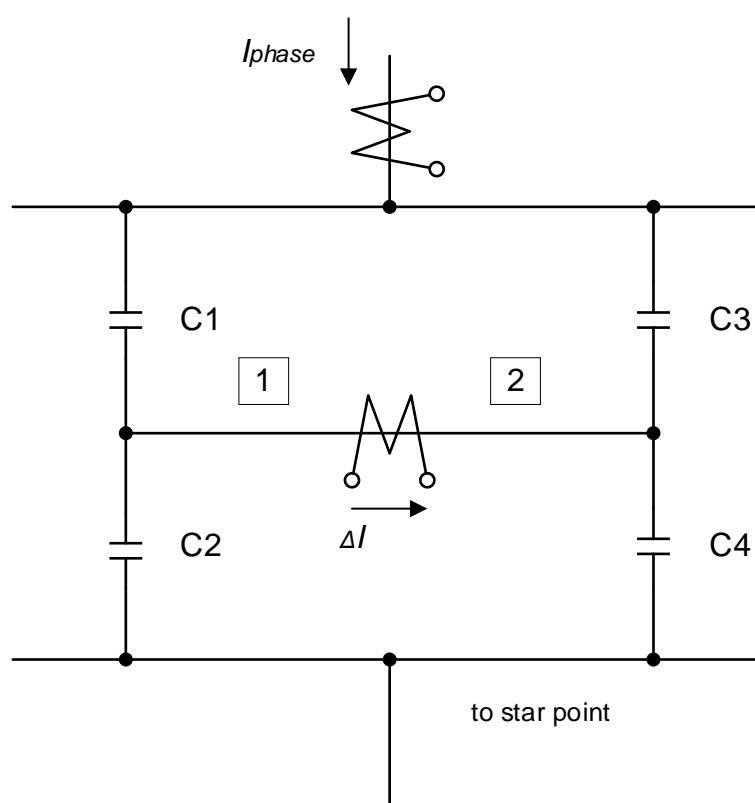


Figure 1-1 Current unbalance in bridge connection ("H configuration")
(drawing in one phase only)

1.2.2 Effect of the "natural" asymmetry of the capacitor bank

The related standard permits a considerable amount of asymmetry, which can be up to 10%, consequently in healthy state a relatively high current can flow through the current transformer. At commissioning the unbalance protection function stores the vector position and the value of the "natural" unbalance currents as three reference currents ΔI_{ref} and additionally those of one of the phase currents $I_{phase_ref} (= IL1)$.

The reference currents are corrected according to the actually measured phase current I_{phase} and the stored I_{phase_ref} reference phase current.

$$\Delta I_{ref_corr} = \Delta I_{ref} \frac{I_{phase}}{I_{phase_ref}}$$

where all current values are complex Fourier base harmonic vectors:

ΔI_{ref}	reference current measured in the bridge of all three phases at commissioning,
ΔI_{ref_corr}	corrected reference currents of all three phases,
I_{phase}	measured phase current of one of the three phases ($IL1$),
I_{phase_ref}	phase current of one of the three phases measured at commissioning ($IL1$).

The correction is performed with one phase current in all three phases separately.

NOTE: This approach using a single phase current supposes that the asymmetry of the network itself does not change, or the changes are cleared with high speed by other protection functions. If considerable steady-state changes in the symmetry of the network are expected, then the measurement and correction based a single phase current is not sufficient. In this case, please consult Protecta Co. Ltd. for a solution.

1.2.3 The energizing quantity (G)

If there are no changes inside the capacitor then no change can be detected in the actually measured unbalance current related to the corrected reference current.

Accordingly, the energizing quantity for evaluation is the difference of the measured currents in the bridges and the corrected reference current:

$$G = dI = \Delta I - \Delta I_{ref_corr}$$

where all current values are complex Fourier base harmonic vectors:

ΔI	currents measured in the bridge,
ΔI_{ref_corr}	corrected reference currents (see above).

NOTE: The correction is performed in all three phases separately with one phase current.

1.3 Calibration at commissioning

This is the task of the commissioning to store the reference values for the bridge currents ΔI_{ref} , and that of one of the phase currents I_{phase_ref} in the memory.

For this purpose, the function block has a dedicated binary input: Calib. This input must be activated for the calibration. For the physical means for activation see the description of the configuration. This input may be programmed by the user using the graphic logic editor.

The calibration at the moment of activation can be performed only if the conditions for calibration are fulfilled. The conditions for calibration are:



- The phase currents must be less than $2 \cdot I_n$ of the current input,
- The phase currents must be above 70% of the rated capacitor current,
- The bridge currents must be less than the value set by the dedicated parameter.

The calibrated state is indicated by the dedicated binary output of the function Calibrated. This output gets in “true” state only if the calibration procedure in all three phases was successful.

The calibration values are stored in non-volatile memory, separately for each parameter set.

The Reset binary input resets the calibrated state.

Among the “on-line” information the function continuously displays the ΔI currents measured in the bridges. At the moment of calibration these vectors reset to zero vector. See Figure 1-2. At the same time the “Calibrated” field on the screen displays a check-mark. If, however, after calibration any changes happen within the capacitor bank then the displayed values change.

[-] CAPACITOR UNBALANCE		
dI L1	0.00	A
dIL1-IL1 angle	0	deg
dI L2	0.00	A
dIL2-IL1 angle	0	deg
dI L3	0.00	A
dIL3-IL1 angle	0	deg
Cap. Fault location	N/A	
Calibrated	<input type="checkbox"/>	
Start Stage1 L1	<input type="checkbox"/>	
Trip Stage1 L1	<input type="checkbox"/>	
Start Stage1 L2	<input type="checkbox"/>	
Trip Stage1 L2	<input type="checkbox"/>	
Start Stage1 L3	<input type="checkbox"/>	
Trip Stage1 L3	<input type="checkbox"/>	
Start Stage2 L1	<input type="checkbox"/>	
Trip Stage2 L1	<input type="checkbox"/>	
Start Stage2 L2	<input type="checkbox"/>	
Trip Stage2 L2	<input type="checkbox"/>	
Start Stage2 L3	<input type="checkbox"/>	
Trip Stage2 L3	<input type="checkbox"/>	
dI123 Current input assignment	Complete	
Iref Current input assignment	Complete	

Figure 1-2 On-line display of the “ $dI=\Delta I$ ” neutral current, referred to the reference current

1.4 Operating characteristics

The capacitor unbalance protection function is configured with two independent stages.

For the first stage definite time characteristic and several types of inverse characteristics can be selected.

The second stage has a definite time characteristic.

1.4.1 Definite time characteristic

$$t(G) = t_{OP} \text{ when } G > G_S$$

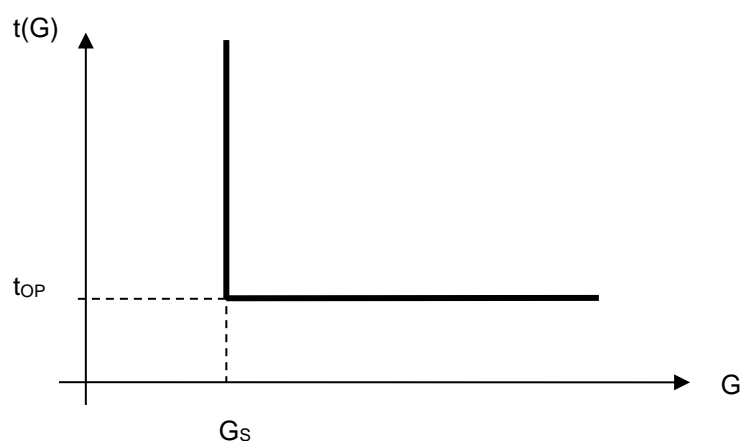


Figure 1-3 Overcurrent definite time characteristic

Where

t_{OP} (seconds)	theoretical operating time if $G > G_S$, fix, according to the preset parameter,
G	measured value of the characteristic quantity, Fourier base harmonic value, see section 1.2.3,
G_S	preset starting value of the characteristic quantity.

1.4.2 Standard inverse time characteristics

Operating characteristics:

$$t(G) = TMS \left[\frac{k}{\left(\frac{G}{G_S}\right)^\alpha - 1} + c \right] \text{ when } G > G_S$$

Where

$t(G)$ (seconds)	theoretical operate time with constant value of G ,
k, c	constants characterizing the selected curve (in seconds),
α	constants characterizing the selected curve (no dimension),
G	measured value of the characteristic quantity, Fourier base harmonic value, see section 1.2.3,
G_S	preset starting value of the characteristic quantity,
TMS	preset time multiplier (no dimension).

Table 1-1 The constants of the standard dependent time characteristics

	IEC REF	TITLE	K_R	c	α
1	A	IEC Inv	0,14	0	0,02
2	B	IEC VeryInv	13,5	0	1
3	C	IEC ExtInv	80	0	2
4		IEC LongInv	120	0	1
5		ANSI Inv	0,0086	0,0185	0,02
6	D	ANSI ModInv	0,0515	0,1140	0,02
7	E	ANSI VeryInv	19,61	0,491	2
8	F	ANSI ExtInv	28,2	0,1217	2
9		ANSI LongInv	0,086	0,185	0,02
10		ANSI LongVeryInv	28,55	0,712	2
11		ANSI LongExtInv	64,07	0,250	2

The end of the effective range of the inverse time characteristics (G_D) is:

$$G_d = 20 * G_S$$

Above this value the theoretical operating time is definite:

$$t(G) = TMS \left[\frac{k}{\left(\frac{G_D}{G_S}\right)^\alpha - 1} + c \right] \text{ when } G > G_D = 20 * G_S$$

Additionally, a minimum time delay can be defined by parameter setting. This delay is valid if it is longer than $t(G)$, defined by the formula of the operating characteristics above.

The inverse characteristic is valid above $G_T = 1,1 * G_S$. Above this value the function is guaranteed to operate.

Resetting characteristics:

- For IEC type characteristics the resetting is after a fix time delay defined by the parameter CapUnB3_Reset_TPar_ (Reset Time),
- for ANSI types however according to the formula below:

$$t_r(G) = TMS \left[\frac{k_r}{1 - \left(\frac{G}{G_S}\right)^\alpha} \right] \text{ when } G > G_S$$

Where

$t_r(G)$ (seconds)	theoretical reset time with constant value of G ,
k_r	constants characterizing the selected curve (in seconds),
α	constants characterizing the selected curve (no dimension),
G	measured value of the characteristic quantity, Fourier base harmonic, see section 1.2.3,
G_S	preset value of the characteristic quantity (CapUnB3_StCurr1_IPar_, Start current 1),
TMS	preset time multiplier (no dimension).

Table 1-2 The resetting constants of the standard dependent time characteristics

	IEC REF	TITLE	K_R	α
1	A	IEC Inv	Resetting after fix time delay, according to preset parameter CapUnB3_Reset_TPar_ "Reset Time"	
2	B	IEC VeryInv		
3	C	IEC ExtInv		
4		IEC LongInv		
5		ANSI Inv	0,46	2
6	D	ANSI ModInv	4,85	2
7	E	ANSI VeryInv	21,6	2
8	F	ANSI ExtInv	29,1	2
9		ANSI LongInv	4,6	2
10		ANSI LongVeryInv	13,46	2
11		ANSI LongExtInv	30	2

1.5 Fault location

The vector measurement enables identification of the faulty capacitor unit. For the explanation of the principle of fault location consider the positive direction of the current I_{phase} and ΔI as indicated in Figure 1-1: the current flows from capacitor unit 1 to capacitor unit 2.

Now consider a fault in phase L1, inside unit 1 in the capacitor C1, which increases the capacitance value, consequently, decreases the impedance related to the impedance of C3. The current in C1 increases related to the current of C3, consequently the current flows in the bridge from the unit 1 towards the unit 2. It is obvious that this current is in phase with the current of the original phase capacitor "IL1", as it is indicated in Figure 1-4. Consequently the ΔI current measured in the bridge is in phase with the current of the original phase capacitor. To permit some asymmetry changes in the network and some measuring error, this current is inside the shaded area between -15° and $+15^\circ$. The on-line measurement will display the increased "dI" value with "dI-IL1 angle" in this range. The related event indicates "L1-1". The same current vector flows in the bridge if the value of the capacitor 4 increases, here the event should be "L1-4". Based on the current measurement these two events cannot be separated so the common fault identification is: "L1-1 or L1-4"

If the capacitor elements are not fused, then the breakdown of a capacitor element will short-circuit a "layer" of capacitors. The capacitance increases and consequently also the capacitive current increases. This case was described in the explanation above.

If, however, the capacitor elements are individually fused then the breakdown of a capacitor element is disconnected from the "layer" of capacitors. The resultant capacitance decreases, and the result is opposite to the explanation in Figure 1-4.

For correct evaluation the information is needed: whether internal fuses are applied or not. This is to be set by the Boolean parameter "Internal fuse".

The event list related to the capacitor faults can contain the following messages:

Table 1-3 Capacitor fault location

MESSAGE	EXPLANATION
L1-1 or L1-4	Fault in phase L1, C1 or C4
L2-1 or L2-4	Fault in phase L2, C1 or C4
L3-1 or L3-4	Fault in phase L3, C1 or C4
L1-2 or L1-3	Fault in phase L1, C2 or C3
L2-2 or L2-3	Fault in phase L2, C2 or C3
L3-2 or L3-3	Fault in phase L3, C2 or C3

NOTE: The fault location is active in "Calibrated" state only. The event is registered at the moment of trip command generation.

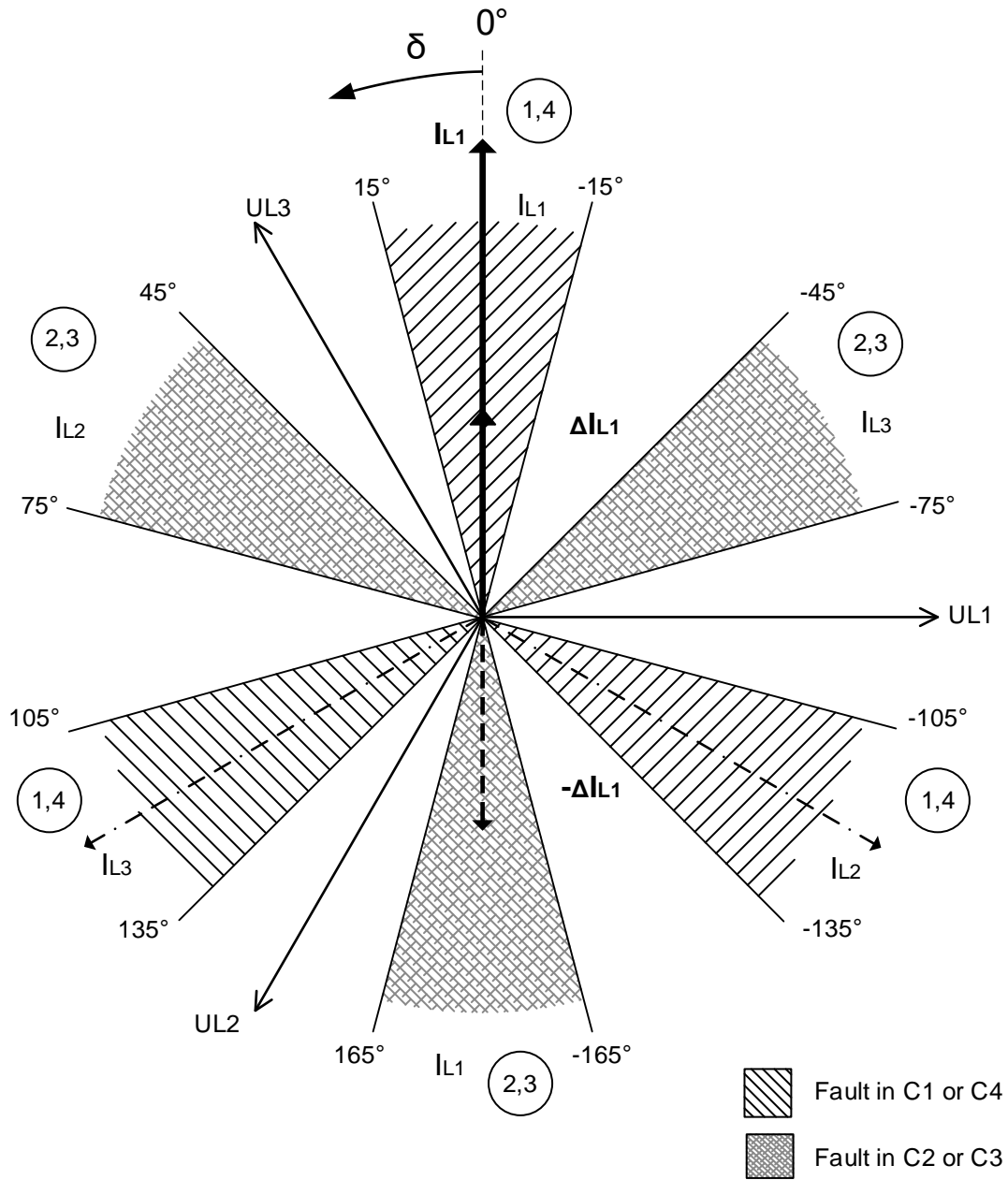


Figure 1-4 Scheme of the fault location

2 Overview

The function block of the capacitor unbalance protection function is shown in Figure 2-1. This block shows all binary input and output status signals that are applicable in the graphic logic editor.

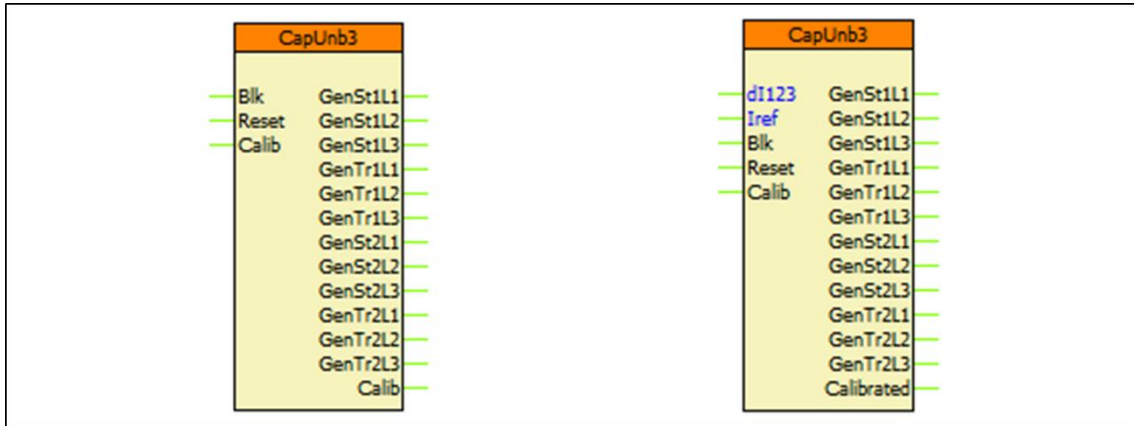


Figure 2-1 The function block of the capacitor unbalance protection function

2.1 Settings

2.1.1 Parameters

The parameters are listed as they are seen on the local or remote HMI.

Table 2-1 Parameters of the capacitor unbalance protection function

TITLE	DIM	RANGE	STEP	DEFAULT	EXPLANATION
Internal fuse	-	FALSE, TRUE	-	FALSE	FALSE means no internal fuse TRUE means capacitor units with internal fuse
Rated Current	%	15 - 120	1	100	Nominal current of the capacitor, as percent of the rated input current
Max dI at Calibration	%	5 - 50	1	10	ΔI setting, at calibration the current between the neutral points must be below this level
Operation Stage 1	-	Off, DefinitTime, IEC Inv, IEC VeryInv, IEC ExtInv, IEC LongInv, ANSI Inv, ANSI ModInv, ANSI VeryInv, ANSI ExtInv, ANSI LongInv, ANSI LongVeryInv, ANSI LongExtInv	-	Off	Enabling or disabling the capacitor unbalance protection function
Start Current 1	%	1 - 100	1	10	Current setting for the capacitor unbalance protection function, first stage

Time Multiplier		0.05 – 15.00	0.01	1.00	Time multiplier setting for the inverse type characteristics
Min Time Delay	msec	40 - 60000	1	100	Minimum time delay for the inverse type characteristics (valid, if this characteristic is selected)
Definite Time Delay 1	msec	40 - 60000	1	1000	Definite time delay for the first stage (valid, if this characteristic is selected)
Reset Time	msec	50 - 60000	1	100	Reset time setting, first stage
Operation Stage2	-	Off,On	-	Off	Enabling or disabling the capacitor unbalance protection function
Start Current 2	%	1 - 100	1	10	Current setting for the capacitor unbalance protection function, second stage
Definite Time Delay 2	msec	40 - 60000	1	1000	Definite time delay for the second stage

2.2 Function I/O

This section describes briefly the analogue and digital inputs and outputs of the function block.

2.2.1 Analogue inputs

Graphic Analogue inputs (*only from firmware version 2.10.2.3010 and up*)

The sources of the analogue inputs are defined by the user, applying the graphic equation editor (*Logic Editor*). Parts written in **bold** are seen on the left side of the function block in the Logic editor.

The function uses the following analogue signals as inputs:

Table 2-2 Analogue input signals of the capacitor unbalance protection function

ANALOGUE INPUT SIGNAL	SIGNAL TITLE	EXPLANATION
CapUnB3_ dI123 _AnIn_	Bridge current group	Input for the differential (unbalance) currents
CapUnB3_ Iref _AnIn_	Reference current	Input for the phase current

The applied analogue connectors must be identical to the analogue input type (i.e. voltage to voltage input etc.), Invalid connections are not allowed.

2.2.2 Analogue outputs

The function has no analogue output signals.

2.2.3 Binary input signals (graphed output statuses)

The conditions of the inputs are defined by the user, applying the graphic equation editor (logic editor). The part written in **bold** is seen on the function block in the logic editor.

Table 2-3 The binary input status signals of the capacitor unbalance protection function

BINARY INPUT SIGNALS	EXPLANATION
CapUnB3_ Blk _GrO_	Blocking input
CapUnB3_ Reset _GrO_	Resetting the calibrated state
CapUnB3_ Calib _GrO_	Binary input for calibration

2.2.4 Binary output signals (graphed input statuses)

The binary output status signals of the capacitor unbalance protection function. Parts written in **bold** are seen on the function block in the logic editor.

Table 2-4 The binary output status signals of the capacitor unbalance protection function

BINARY OUTPUT SIGNALS	SIGNAL TITLE	EXPLANATION
CapUnB3_ GenSt1L1 _Grl_	Start Stage1 L1	General Start signal for Stage 1 phase L1
CapUnB3_ GenTr1L1 _Grl_	Trip Stage1 L1	General Trip command for Stage 1 phase L1
CapUnB3_ GenSt2L1 _Grl_	Start Stage2 L1	General Start signal for Stage 2 phase L1
CapUnB3_ GenTr2L1 _Grl_	Trip Stage2 L1	General Trip command for Stage 2 phase L1
CapUnB3_ GenSt1L2 _Grl_	Start Stage1 L2	General Start signal for Stage 1 phase L2
CapUnB3_ GenTr1L2 _Grl_	Trip Stage1 L2	General Trip command for Stage 1 phase L2
CapUnB3_ GenSt2L2 _Grl_	Start Stage2 L2	General Start signal for Stage 2 phase L2
CapUnB3_ GenTr2L2 _Grl_	Trip Stage2 L2	General Trip command for Stage 2 phase L2
CapUnB3_ GenSt1L3 _Grl_	Start Stage1 L3	General Start signal for Stage 1 phase L3
CapUnB3_ GenTr1L3 _Grl_	Trip Stage1 L3	General Trip command for Stage 1 phase L3
CapUnB3_ GenSt2L3 _Grl_	Start Stage2 L3	General Start signal for Stage 2 phase L3
CapUnB3_ GenTr2L3 _Grl_	Trip Stage2 L3	General Trip command for Stage 2 phase L3
CapUnB3_ Calibrated _Grl_	Calibrated	TRUE, if the function has been calibrated

2.2.5 On-line data

Visible values on the on-line data page:

Table 2-5 The displayed on-line data of the capacitor unbalance protection function

SIGNAL TITLE	DIMENSION	EXPLANATION
dI L1	A	Magnitude of the measured unbalance current in phase L1.
dIL1-IL1 angle	deg	Angle of the differential current related to the L1 phase current.
dI L2	A	Magnitude of the measured unbalance current in phase L2.
dIL2-IL1 angle	deg	Angle of the differential current related to the L1 phase current.
dI L3	A	Magnitude of the measured unbalance current in phase L3.
dIL3-IL1 angle	deg	Angle of the differential current related to the L1 phase current.
Cap. Fault location	N/A, L1-1orL1-4, L1-2orL1-3, L2-1orL2-4, L2-2orL2-3, L3-1orL3-4, L3-2orL3-3	The detected location of the fault given in pairs [phase]-[bankA]or[phase]-[bankB]
Calibrated	Off,On	TRUE, if the function has been calibrated
Start Stage1 L1	Off,On	General Start signal for Stage 1 phase L1
Trip Stage1 L1	Off,On	General Trip command for Stage 1 phase L1
Start Stage1 L2	Off,On	General Start signal for Stage 1 phase L2
Trip Stage1 L2	Off,On	General Trip command for Stage 1 phase L2
Start Stage1 L3	Off,On	General Start signal for Stage 1 phase L3
Trip Stage1 L3	Off,On	General Trip command for Stage 1 phase L3
Start Stage2 L1	Off,On	General Start signal for Stage 2 phase L1
Trip Stage2 L1	Off,On	General Trip command for Stage 2 phase L1
Start Stage2 L2	Off,On	General Start signal for Stage 2 phase L2
Trip Stage2 L2	Off,On	General Trip command for Stage 2 phase L2
Start Stage2 L3	Off,On	General Start signal for Stage 2 phase L3
Trip Stage2 L3	Off,On	General Trip command for Stage 2 phase L3
<i>dI123 Current input assignment</i>		<i>Status of the graphical analogue input (if exists) (Complete if OK, Missing if not connected)</i>
<i>Iref Current input assignment</i>		<i>Status of the graphical analogue input (if exists)</i>

2.2.6 Events

The following events are generated in the event list, as well as sent to SCADA according to the configuration.

Table 2-6 Events of the capacitor unbalance protection function

EVENT	VALUE	EXPLANATION	IEC61850 DATA ATTRIBUTES (SYSTEM 2.8)	IEC61850 DATA ATTRIBUTES (SYSTEM 2.10)
Start Stage 1	Off,On	General Start signal for Stage 1	F3PTOC1\$ST\$Str	CUNBPTOC3\$ST\$Str
Start Stage 2	Off,On	General Start signal for Stage 2	F3PTOC2\$ST\$Str	CUNBPTOC4\$ST\$Str
Trip Stage 1	Off,On	General Trip signal for Stage 1	F3PTOC1\$ST\$Op	CUNBPTOC3\$ST\$Op
Trip Stage 2	Off,On	General Trip signal for Stage 2	F3PTOC2\$ST\$Op	CUNBPTOC4\$ST\$Op
Start Stage1 L1	Off,On	General Start signal for Stage 1 phase L1	F3PTOC1\$ST\$Str\$phsA	CUNBPTOC3\$ST\$Str\$phsA
Start Stage2 L1	Off,On	General Start signal for Stage 2 phase L1	F3PTOC2\$ST\$Str\$phsA	CUNBPTOC4\$ST\$Str\$phsA
Start Stage1 L2	Off,On	General Start signal for Stage 1 phase L2	F3PTOC1\$ST\$Str\$phsB	CUNBPTOC3\$ST\$Str\$phsB
Start Stage2 L2	Off,On	General Start signal for Stage 2 phase L2	F3PTOC2\$ST\$Str\$phsB	CUNBPTOC4\$ST\$Str\$phsB
Start Stage1 L3	Off,On	General Start signal for Stage 1 phase L3	F3PTOC1\$ST\$Str\$phsC	CUNBPTOC3\$ST\$Str\$phsC
Start Stage2 L3	Off,On	General Start signal for Stage 2 phase L3	F3PTOC2\$ST\$Str\$phsC	CUNBPTOC4\$ST\$Str\$phsC
Cap Fault location	N/A, L1-1orL1-4, L1-2orL1-3, L2-1orL2-4, L2-2orL2-3, L3-1orL3-4, L3-2orL3-3	The detected location of the fault given in pairs: [phase]-[bankA] or [phase]-[bankB]	FLGGIO2\$ST\$IntIn	CAPFLGGIO2\$ST\$IntIn

2.3 Technical data

Table 2-7 Technical data of the unbalance protection function

FUNCTION	VALUE	ACCURACY
Pick-up starting accuracy	$20 \leq G_s \leq 1000$	< 5 %
Pickup time	< 40 ms	
Angle accuracy		<1 degree
Reset ratio	0,9	
Reset time Dependent time char. Definite time char.	Approx 60 ms	< 2% or ± 35 ms, whichever is greater
Operate time accuracy		$\pm 5\%$ or ± 15 ms, whichever is greater

2.3.1 Notes for testing

When calibrating the function, take note of the dl measurements that have been nullified: those unbalance values must be taken into consideration when testing the calibrated function.

Normally in the EuroProt+ devices the trip contacts are assigned to the Trip Logic function block, and not to the protection function blocks. Because of this the testing personnel must make sure that the Trip Logic is switched on ('Operation' parameter is set to other than 'Off') before starting the testing, otherwise there will be no physical trip on the relay.

Additional notes for Graphic Analogue inputs (*only from firmware version 2.10.2.3010 and up*):

Starting from the firmware version **2.10.2.3010**, the majority of the function blocks can be updated to be equipped with graphic analogue inputs which **allow the user to assign the functions' analogue inputs by applying the graphic equation editor**.

The analogue connections of these functions can be checked by examining the source that is connected to their inputs (just like examining the source of a logic signal).

These functions must be placed in the Logic Editor and their graphic analogue inputs must be connected to make them operate. If a connection is intact, the online status of the corresponding analogue input will show "Complete". If it is missing, the status will be "Missing" and the function will not operate.



Note that these graphical inputs do not exist in the earlier firmware/function versions! Checking and modifying the analogue assignments in these cases are done by using the EuroCAP Software Configuration menu.